Tec Empresarial
P-ISSN: 1659-2395; E-ISSN: 1659-3359

EXAMINING CTS CMOS CHARGE PUMP IN LOW VOLTAGE DEVICES FOR HIGH EFFICIENCY

Sakshi Rajput[1], Yash Mani Prakash[2]

Department of Electronics and Communications Engineering

Maharaja Surajmal Institute of Technology, Janakpuri

GGSIPU, New Delhi, India

Abstract-Circuits known as charge pumps produce voltages greater than the voltage supplied needed to power them. Although the circuit is basic, charge pump circuits can achieve high efficiencies of up to 90–95%. To completely minimize the impact of threshold voltage during each pumping stage in these type of pump, MOS transistors will be used as switches to charge transfer. No additional circuitry for this as the output of dynamic inverter controls the CMOS switch in every pumping stage to reduce the possibility of reverse current. Nowadays machine learning and artificial intelligence models could be implemented in CMOS chips.

Keywords: DC to DC converter, Dynamic pump, Dickson pump, Charge pump, Static charge pump.

1. Introduction

Charge pumps are a type of DC to DC converter that produce either a higher or lower voltage power source by using capacitor as energy storage components. When voltages that are either greater or lower than the power source voltage are needed, charge pumps are employed. Charge pumps transform lower input DC voltage levels to higher output DC voltage levels. using switches to pump charges toward the output stage. Capacitors are used as the energy storage component in charge pumps. These circuits are useful for programming floating gate devices in nonvolatile storage like EEPROM and Flash. Research into revolutionary nanodevices that perform new functionalities like large-scale vector matrix multiplication or synaptic weighing and neural response is speeding up due to the rapid emergence of artificial intelligence and so its unquenchable need for low-energy, high performance computing. Complementary metal oxide semiconductor (CMOS) electronics must be integrated into experimental devices in order to assess the performance of these functions.

1.1 Why Low Voltage CMOS Charge-Pump DC-DC Converters Are Needed

It would be advantageous to create a DC-DC converter in CMOS. At the moment, CMOS is the preferred technology for low power design. The simplicity of building circuits with low static power dissipation is a major factor in CMOS's popularity. The body effect has been eliminated by

the circuit of CMOS charge pump thats employs both NMOS and PMOS switches. To achieve high voltage, gain, an unique CTS control technique that combines both the forward and backward control scheme have been used. According to the simulated results, the CMOS charge pump can achieve a significantly greater pumping efficiency in the 180nm CMOS process than existing charge pumps.

2. Implementation

The dc-dc conversion circuit called a charge pump is used to produce dc voltage which will be one of the two, lower or higher than the input voltage or polarity opposite to the input voltage. The critical factors that must be taken into account while designing on chip charge pump circuits are covered in this thesis. The output voltage ripple is one crucial concern. The majority of applications call for a output ripple to reduce. If the output value of ripple is very large, the charge pump's powered circuit performs poorly. Power efficiency is a further key factor. Very inefficient charge pumps lose too much energy to be useful for portable applications. Area efficiency is another problem. It is preferable to reduce the amount of space on the chip.

The development of AI has benefited from developments in chip technology, graphic processing units, sensors, communications systems, etc. Engineering in electronics and communication is crucial to these. The investigators provided artificial intelligence (AI) strategies in the expanding field of Chip design in the VLSI and automation sector to solve challenges at various development and construction phases. Similar to knowledge-based and skilled systems, AI methods first attempt to state the issue before choosing the best outcome from a field of potential solutions. The development of the ever-evolving VLSI technology and the transition from the designing of Semiconductor wafers towards the Ultra Large Scale Integrated circuit systems have occurred quickly and extraordinarily thanks to the incorporation and involvement of the most recent design automation tools. The computerization of VLSI design was further enhanced by the utilization of computer-aided design and software tools.

2.1 **Dickson pump**

The coupling capacitors in the Dickson pump circuit must be able to sustain the entire output voltage because they are parallel connected. As the number of stages goes on increasing, the output impedance decreases as a result. It may be demonstrated that both circuits are equivalent and call for the same amount of diodes and capacitors. For producing greater voltages, the Dickson pump circuit seen in Figure 2 is commonly used. Instead of using p-n junction diodes, diode-connected NMOS devices were used to build the circuitry in a traditional CMOS process. In a perfect world, only charge can travel in the path of the output terminal through the diode-connected NMOS. The resultant DC voltage rises when the charges are transferred from one step to the next.

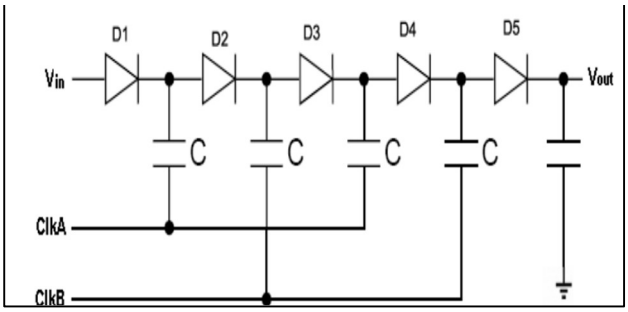

Figure 1: Four stage Dickson pump

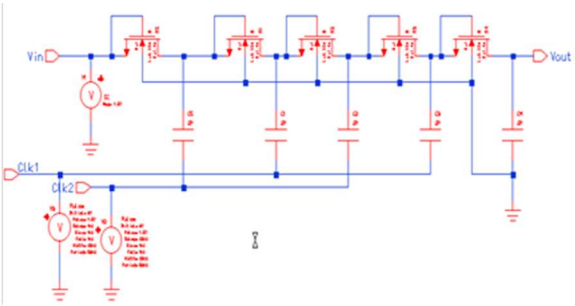

Figure 2: Four stage Dickson pump (schematic)

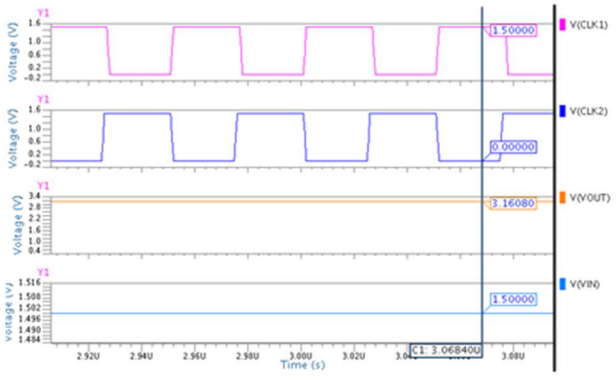

Figure 3: Output waveform of Four stage Dickson pump

Dickson pump circuit's disadvantage is that the threshold drops across the diodes cause the boosting ratio to be reduced by a factor of 3. At higher voltages, the body effect exacerbates this issue.

2.2 **Static Charge Pump**

To prevent the threshold decrease, charge transfer switches are used in combination to transistors coupled to diodes.

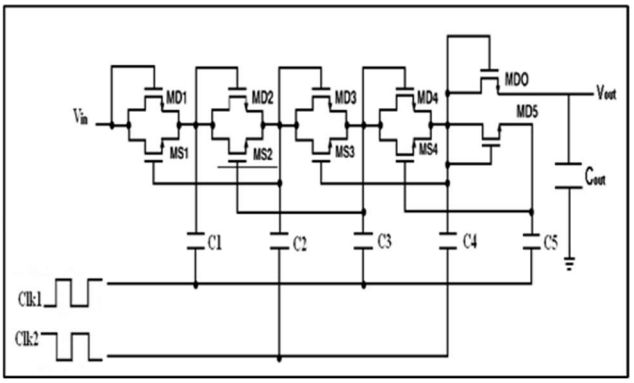

Figure 4: Four stage Static Charge Pump

New charge pumps called static CTS charge pumps use dynamic switches which boost voltage pumping gain. The fundamental concept of a multiplier is to avoid utilizing diodes or transistors coupled to diodes, which invariably result in a forward voltage drop at each node, by using CMOS gates with exact on/off properties to regulate charge flow while pumping.

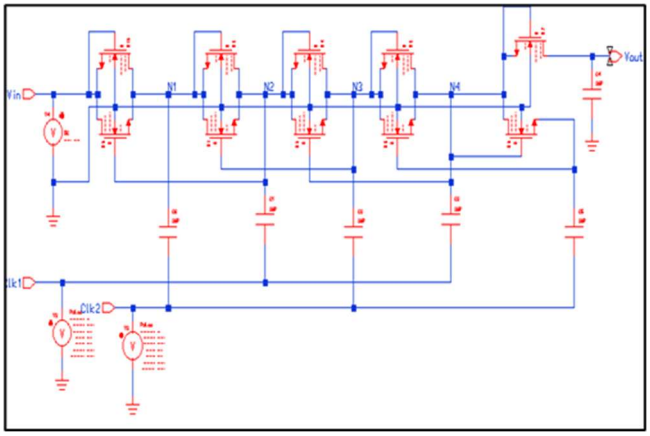

Figure 5: Static charge 4 stage schematic

The Dickson pump is significantly less effective at pumping charge than the Static Charge pump.

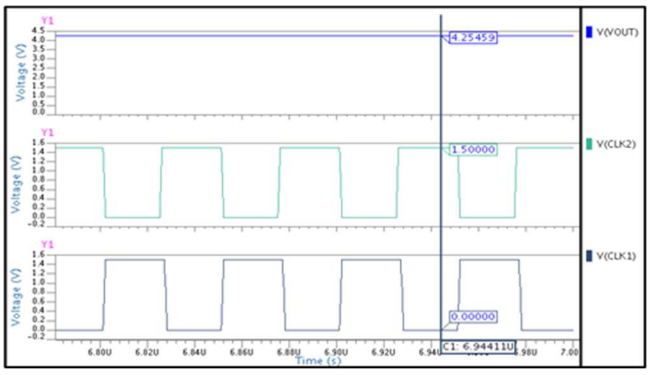

Figure 6: Output waveform of Four stage Static charge pump

This circuit design does have a minor flaw, especially opposite way charge leakage. When clock1 is low, at nodes 2 and 3, the voltage is equal to and higher than node 1 voltage. By including pass transistors in the Static charge pump circuit (both NMOS and PMOS), this reverse charge leaking phenomena can be stopped. These transistors have the purpose of applying dynamic control to the CTSs so that they can be entirely turned off when necessary while yet being easily turned on by the reverse controlling voltage like in this case of a static charge pump.

2.3 **Dynamic Pump**

Low-voltage circuits are intended to use this charge pump and is an updated design that solves the prior issue by including pass transistors to the prior circuit (Figure 7). Transceivers also employ charge pump voltage boosters.

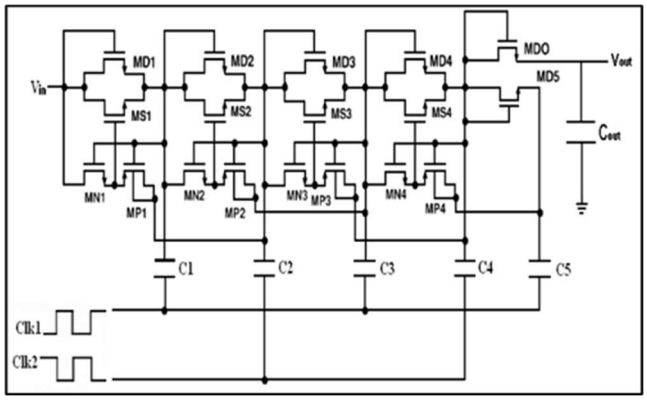

Figure 7: 4-stage Dynamic Pump

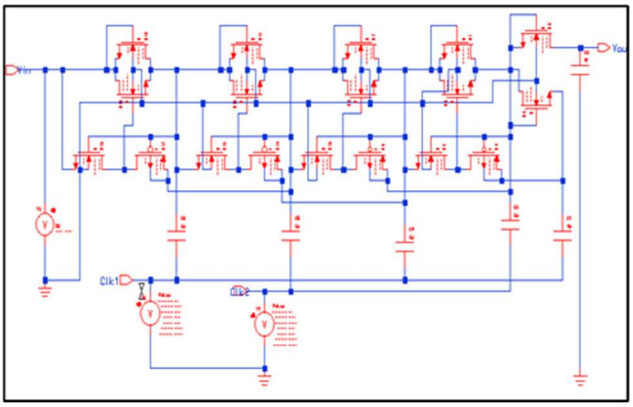

Figure 8: Four stage Dynamic pump (schematic)

In this circuit design, CTS are used as dynamic charge transfer switch. The PT (pass transistors) MN's and MP's regulate each of the CTS (MS's transistors). Usage of dynamic CTS allows for the transfer of charges between stages without encountering the issue of Vth voltage drop. When necessary, the CTSs could be entirely turned off; also, the higher voltage produced in the following stages can be used to effectively turn the CTSs on. As a result, reverse charge flow is prevented,

increasing efficiency. In ideal circumstances, a 4-stage Dynamic pump's output voltage should be 5 times VDD.

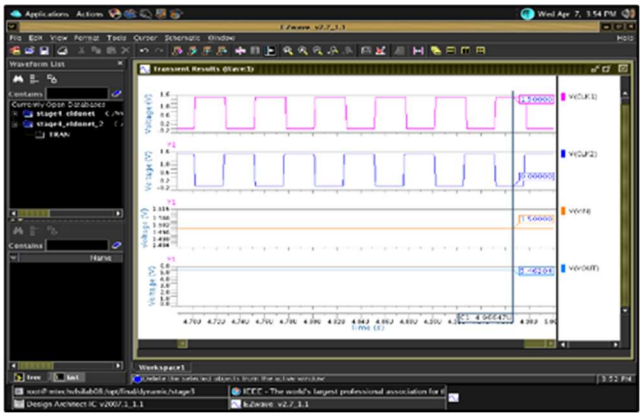

Figure 9: Output waveform of Four stage Static charge pump

2.4 CMOS Charge Pump with High Performance for Low Voltage Operations

In order to improve pumping efficiency when operating at low voltage, charge pump circuitry with such a unique CTS control method is being developed. PMOS CTS forward control and the NMOS CTS backward control of are both used in the new CTS control method. During dynamic control, the NMOS CTS does not have any substrate current, and the PMOS CTS effectively cancels out the body effect of the output. With this charge pump circuit, excellent pumping efficiency and dependability can be attained.

By managing backward control by NMOS and forward control by PMOS, the unique CTS control technique is created to improve pumping efficiency. The NMOS switch is regulated by a high voltage that is derived from this stage after it in a backward control scheme, and PMOS switch is regulated by a low voltage that is derived from the stage before it in a forward control scheme.

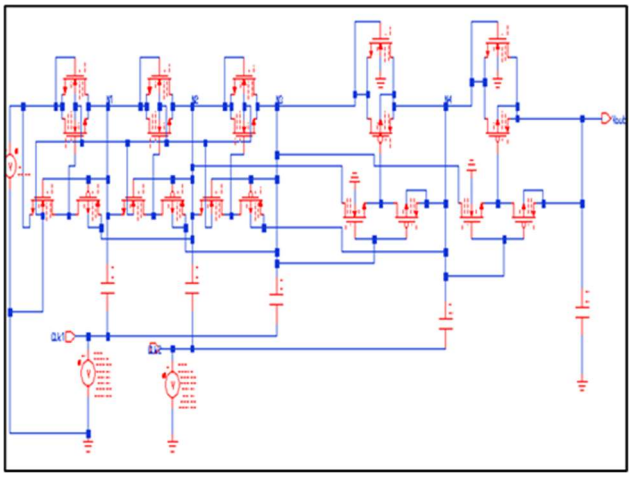

Figure 10: 4-stage High performance CMOS charge pump(schematic)

3. Related Work

A CP circuit with 6 stages and 6 pumping capacitors for each and every pumping node was created by Yan et al. (2012) utilizing an enhanced charge sharing mechanism. Based on the CTS approach, Yan et al. enhanced the efficiency of the charge pump circuitry in this design. The zero Vth MOSFET was also used to get around Vth drop at each node. Additionally, feedback current can be decreased and charge transfer switches could be totally turned on or off. Due to the intricate circuitry, this design squandered a tremendous amount of power with only a few stages.

Wei et al. (2013) introduced an upgraded NCP-2 CTS CP circuit with better voltage pumping gain for the shortest charge flow. A suitable clock method and the sizing of the pumping capacitors were used in this design to overcome the restrictions imposed by the diode configuration. Additionally, the technique also has the lowest levels of parasitic capacitance effects. The system's higher pumping efficiency, increased power dissipation, and low output voltage were negative aspects.

A completely integrated inductor-based CP design method for a DC/DC converter was put up by Zucchelli et al. in 2016. Despite being a modified version of the original Dickson CP circuit, the design performs better because small inductors are used in the charge transfer process' initial stages. Thus, the suggested design can decrease output voltage ripple, rising time, and power dissipation. Additionally, this design was clear of any extraneous parts, which allowed it to work with CMOS technology.

In 2017, Rumberg et al. developed a novel controlled CP circuit that is centered on floating-gate transistors. Applications requiring tunneling voltages to train floating-gate transistors can benefit from this kind of arrangement. Due to its small size, the CP has been able to offer stable tunneling voltages by using variable frequency control and minimized short-circuit current. Power dissipation may be decreased by this design. However, this circuit is not appropriate for uses that require common CMOS transistors.

Using the CP approach, Abdi et al. created a high voltage generator in 2018 that offers different types of programmable clock frequency and voltage regulation. In this layout, an input power modulation is introduced to a low-dropout regulator at the input terminal in order to transmit the input voltage to the following nodes. This method has led to increased output voltage with trustworthy voltage regulation. Thick-oxide transistors were additionally employed in maintaining a stable substrate/n-well voltage level and boosting pumping efficiency throughout the process.

Rahman et al. introduced a redesigned charge transfer switch-based CP circuitry in year 2020 to become congruent with RFID tag EEPROM. Instead of using a diode configuration inside the charge transfer nodes, all NMOS switches are employed in this design. By reducing the substrate current & overall power dissipated, this structure was able to accomplish this. With this method, researchers may also decrease the output chip layout size and ripple voltage. This design also

includes a voltage regulator which produces the steady-boost voltage required for RFID tag memories.

4. Result

Parameters:

a) Pumping Capacitor- 2pf

b) Type of Technology- 180nm

c) Width of transistor- 1.4micron

d) Input Voltage- 1.4V

e) Clock Frequency- 25MHz

Result obtained for Dickson pump

a) Resultant Voltage- 03.1608V

b) Power dissipated- 13.217pW

Result obtained for Static charge pump

a) Resultant Voltage- 3.997V

b) Power dissipated- 24.942pW

Result obtained for Dynamic pump

a) Resultant Voltage- 5.462V

b) Power dissipated- 31.328pW

5. Conclusion

Suggested CMOS charge pump circuit using both NMOS and PMOS switches eliminates the body effect. A different CTS control method that integrates the forward control strategy and the backward control strategy are created to achieve a high voltage gain. According to the simulation results, the proposed charge pump could achieve a much greater pumping performance in the 180nm CMOS technology in comparison to earlier charge pumps.

6. References

[1] G. Palumbo, D. Pappalardo and M. Gaibotti, "Charge- pump circuits: power-consumption optimization," IEEE Transaction on Circuits and systems I, vol. 49, no. 11, pp.1535-1542, Nov. 2002.

[2] "Rajput, S., Bhatia, K.S. Analyzing handover performance of mobility management protocol using neural network. J Ambient Intell Human Comput (2021). https://doi.org/10.1007/s12652-020-02822-1

[3] Kumar, A., Gupta, R., Rajput, S., Bhatia, K.S., Kaur, H. and Gautam, A.K., 2022. Narrow beamwidth conical dielectric resonator antenna. Journal of Optoelectronics and Advanced Materials, 24(March-April 2022), pp.175-186.

[4] T. Tanzawa, T. Tanaka, T. Takeuchi, and K. Nakamura, "Circuit techniques for a 1.8-V-only NAND flash memory," IEEE J. Solid-State Circuits, vol. 37, no. 1, pp. 84-89, Jan.2002.

[5] J.-T. Wu, Y.-H. Chang, and K.-L. Chang, "1.2 V CMOS switched capacitor circuits," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 1996, pp. 388–389.

[6] Jaycar Electronics Reference Data Sheet: DCDCCONV.PDF (1).

[7] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," IEEE J. Solid- State Circuits, vol. 11, pp. 374–378, June 1976.

[8] Y. Nakagome et al., "An experimental 1.5-V 64 Mb DRAM," IEEE Journal of Solid-State Circuits, vol. 26, pp. 465-472, April 1991.

[9] S. Singer,"Inductance-less up dc-dc convertor," IEEE Journal of Solid-State Circuits, vol. SC-17, pp. 778-781, Aug. 1982.

[10] P. Gillingham et al.,"High-speed, high-reliability circuit design for megabit DRAM," IEEE Journal of Solid-State Circuits, vol. 26, pp. 1171-1175, August 1991.

[10] W. Martino et al.,"An on-chip back-bias generator for MOS dynamic memory," IEEE Journal of Solid-State Circuits, vol. SC-15, pp. 820-825, Oct. 1980.

[11] T. Byunghak and P. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," IEEE Journal of Solid-State Circuits, vol. 30, pp. 166-172, March 1995.